

CSE369 Practice Problems (lec 2)

1. Circuit diagrams

Draw a truth table and circuit diagram for each of the following boolean equations

1.1] $X = ABC$

1.2] $X = AB + C$

1.3] $Z = A\bar{B} + \bar{A}B$

2. DeMorgan's Law

2.1.1] Draw this equation as a circuit: $P = \overline{A} + B$

2.1.2] Use “bubble pushing” to convert the circuit diagram to *only* use **NAND** gates

2.1.3] Write the circuit as a boolean equation

2.2.1] Draw this equation as a circuit: $Q = \overline{(A + B)(B + \sim C)}$

2.2.2] Use “bubble pushing” to convert the circuit diagram to *only* use **NOR** gates

2.2.3] Write the circuit as a boolean equation

3. Verilog Signals

3.1] Declare a six bit bus called “twix” and a 16 bit bus called “kitkat”

3.2] Declare a 16 bit bus called “katkit”. Use concatenation to assign its value to be the bytes of “kitkat” in the opposite order.

3.3] Declare a 16 bit bus called “nokit”. Use concatenation to assign its value to be the upper byte of “kitkat” padded out to 16 bits with 0s

3.4] Declare a six bit bus called “xiwt”. Use concatenation to assign its value to be the reversed bits of twix.

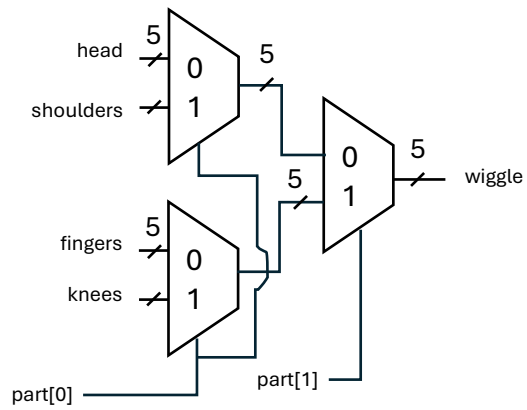
3.5] Declare a three bit bus called “tw” and a three bit bus calle “ix”. Use concatenation on the left side of an assignment to break the value of twix apart into tw and ix.

4. Block diagramming

4.1] Draw the following Verilog as a block diagram:

```
logic [6:0] danni_age;  
logic [6:0] naomi_age;  
logic [6:0] age;  
logic cat_years ;  
always_comb begin  
    if (cat_years) begin  
        age = danni_age;  
    end else begin  
        age = naomi_age;  
    end  
end  
end
```

4.2] Write Verilog for the following block diagram:



4.3] Write Verilog for the following block diagram:

